REMARKS/ARGUMENTS

This Application is in response to the Final Office Action dated February 23, 2005. In the Office Action, claims 1-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Ishac (U.S. Patent No. 5,812,861) in view of Russell (U.S. Patent No. 4,841,492) and Brown (U.S. Patent No. 6,487,667). Applicant respectfully traverses the rejection because *a prima facie* case of obviousness has not been established.

As the Examiner is aware, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify a reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. *See MPEP §2143; see also In Re Fine, 873 F. 2d 1071, 5 U.S.P.Q.2D 1596 (Fed. Cir. 1988).* Herein, at a minimum, the combined teachings of the cited references do not describe or suggest sufficient motivation to modify the cited references and do not describe all the claim limitations.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *See In re Mills,* 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). Applicants respectfully submit that none of the cited references suggest such combination, and in fact, such combination may constitute impermissible hindsight reconstruction.

Herein, Ishac teaches an indicator (325) of override circuitry (320) that, when set, transmits an OVER-RIDE signal to powerdown controller (310). The indicator (325) is configured to indicate when the die is to be placed into powerdown mode independently of any external powerdown signals (PWD#). More specifically, when the indicator (325) is set, the OVER-RIDE signal causes the powerdown controller (310) to ignore any power-up commands from an external powerdown signal (PWD#). When the indicator (325) has not been set, however, the OVER-RIDE signal will not cause powerdown controller (310) to ignore a power-up command. *See col. 6, lines 31-48 of Ishac.* Russell teaches an output disable pin of phase

selector (22), which is used to inhibit an output of any signal by a transmit focus block (12i) and provides no teaching of preventing access to stored information. Brown teaches a remote pass-phrase authentication technique, which is unrelated to the scope of the claimed invention.

Neither Ishac, Russell nor Brown, alone or in any combination, suggests an operation of preventing modification of a representation of a primary pass-phrase (e.g., pass-phrase itself, derivation of the pass phrase, etc.) when the override disable pin is asserted. The "primary pass-phrase" permits access to stored information within the electronic system. Hence, when the override disable pin is asserted, if the user accidentally forgets the pass-phrase, he or she is fully precluded from accessing the stored information which may render the device inoperable.

Rather, when combining the teachings of these references, the resultant combination produces a disable pin that, when set, ignores any subsequent, external power-up commands. There is no operation involved to prevent modification of the pass-phrase as claimed. In other words, the combined teaching do not teach or even suggest the use of a disable pin to prevent access to stored information such as a pass-phrase within the electronic system as set forth in claims 1, 9 and 18.

Moreover, with respect to independent claim 14, neither Ishac, Russell nor Brown, alone or in any combination, suggests an operation of disabling placement of an integrated circuit device of the electronic system into the administrator mode when an override disable pin of the integrated circuit device is asserted prior to assertion of an override pin. As further claimed in claim 14, data stored within the integrated circuit device "can be cleared only when the integrated circuit device is placed in the administrator mode."

Conclusion

Applicant respectfully believes that all claims are in condition for allowance. Allowance of the pending claims is respectfully requested at the Examiner's earliest convenience.

Respectfully submitted,

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Dated: 05/06/2005

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